GALGOTIAS UNIVERSITY

ADMISSION NUMBER												

School of Basic Sciences

Master of Science in Physics
Mid Term Examination - May 2024

Duration : 90 Minutes
Max Marks : 50

Sem II - C1PO204T - Digital Electronics

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

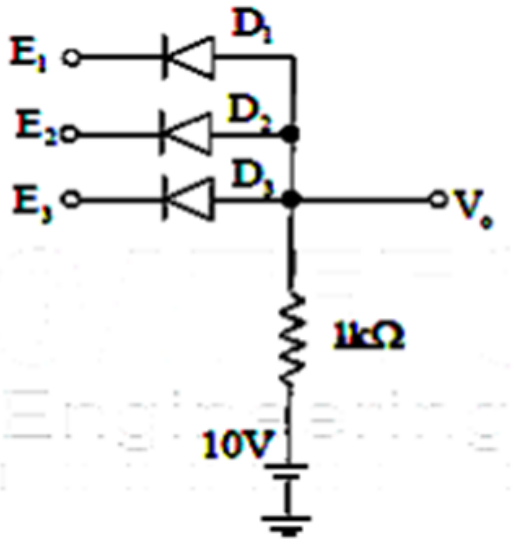
1) Represent — K2 (2)
i) $+(7)_{10}$ & $-(7)_{10}$
ii) $-(8)_{10}$ in 2's complement form

2) Design the Ex-OR gate using NAND gates. — K1 (3)

3) Simply the following Boolean functions using K –Map F(A, B, C, D)=∑m(0,1,3,4,5,7,12,13,15)) — K2 (4)

4) Simply the following Boolean functions using K –Map F (X,Y,Z,W) = Σ (0, 1, 2, 4, 5, 6, 8 , 9 , 12, 13, 14) — K2 (6)

5) Write the name of logic gate of given circuit shown, diodes $D_1, D_2,$ and D_3 are ideal, and the inputs E_1, E_2 and E_3 — K3 (6)



6) Simply the following Boolean functions using K –Map F(A,B,C,D) = Σ (0,2,4,6,9,11,13) — K3 (9)

7)	Write the truth table of full adder and draw the full adder diagram using NAND gates?	K4	(8)
8)	Explain with logic diagram of 4-bit serial-in, serial-out, shift register	K4	(12)
	OR		
	Explain with logic diagram of 4-bit parallel-in, parallel-out, shift register	K4	(12)