Course Code : BSCP3005

Course Name: Digital System and Application

Shift Registers in Digital Electronics and Serial Input Serial Output Registers

Contents:

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Introduction about Register

Flip-flop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a **Register**. The **n-bit register** will consist of **n** number of flip-flop and it is capable of storing an **n-bit** data

Types of registers

The binary data in a register can be moved within the register from one flip-flop to another. The registers that allow such data transfers are called as **shift registers**. There are four mode of operations of a shift register.

Serial Input Serial Output (SISO) Serial Input Parallel Output (SIPO) Parallel Input Serial Output (PISO) Parallel Input Parallel Output (PIPO) The Clear/ input is an active-low asynchronous input which clears the register content to all 0's when asserted low, independent of the clock pulse.

- During normal operation, Clear/ must be maintained at logic 1.
- The transfer of new information into a register is referred to as Loading
- The term Parallel Loading is used if all the input bits are transferred into the register simultaneously, with the common clock pulse.

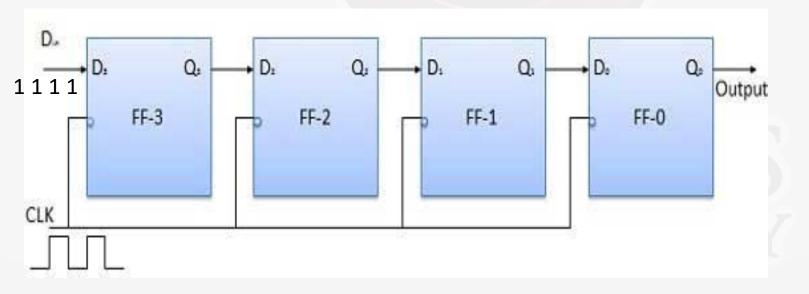
In most digital systems, a master clock generator supplies clock pulses to all parts of the system, just as the heart that supplies a constant beat to all parts in the human system. Because of this fact, the input values in the register are loaded when a clock pulse arrives. This implies that, whenever a clock pulse arrives, it would load the register with new values, thus overwriting the previously stored register data.

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Serial Input Serial Output (SISO) Register

Let all the flip-flop be initially in the reset condition i.e. $Q_3 = Q_2 = Q_1 = Q_0 = 0$. If an entry of a four bit binary number 1 1 1 1 is made into the register, this number should be applied to **D**_{in} bit with the LSB bit applied first. The D input of FF-3 i.e. D₃ is connected to serial data input **D**_{in}. Output of FF-3 i.e. Q₃ is connected to the input of the next flip-flop i.e. D₂ and so on.

Block Diagram

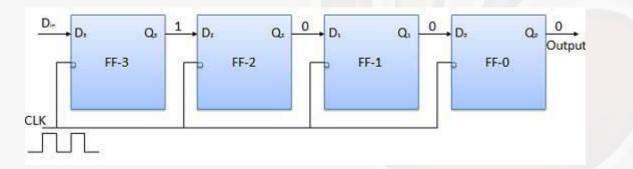


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Before application of clock signal, let $Q_3 Q_2 Q_1 Q_0 = 0000$ and apply LSB bit of the number to be entered to D_{in}. So D_{in} = D₃ = 1. Apply the clock. On the first falling edge of clock, the FF-3 is set, and stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1000$.



Apply the next bit to D_{in} . So $D_{in} = 1$. As soon as the next negative edge of the clock hits, FF-2 will set and the stored word change to $Q_3 Q_2 Q_1 Q_0 = 1100$.

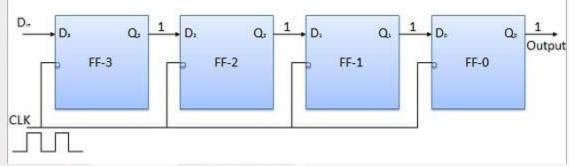
Apply the next bit to be stored i.e. 1 to D_{in}. Apply the clock pulse. As soon as the third negative clock edge hits, FF-1 will be set and output will be modified to $Q_3 Q_2 Q_1 Q_0 = 1110$.

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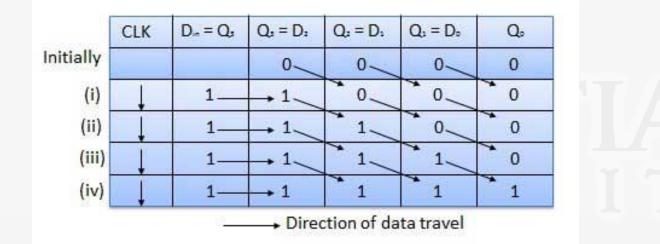
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Similarly with $D_{in} = 1$ and with the fourth negative clock edge arriving, the stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1111$



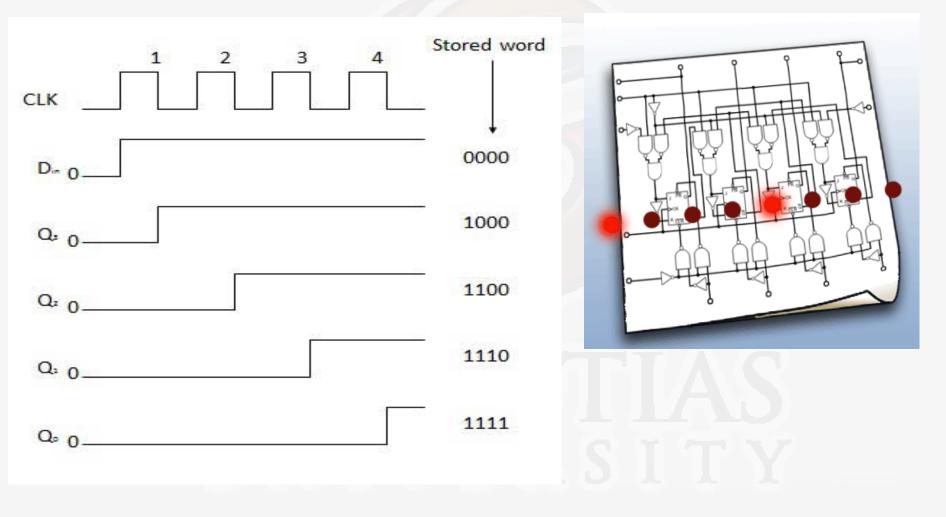
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Waveforms



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Applications

sometimes it's necessary to send or receive data serially, or one bit at a time. Some examples include:

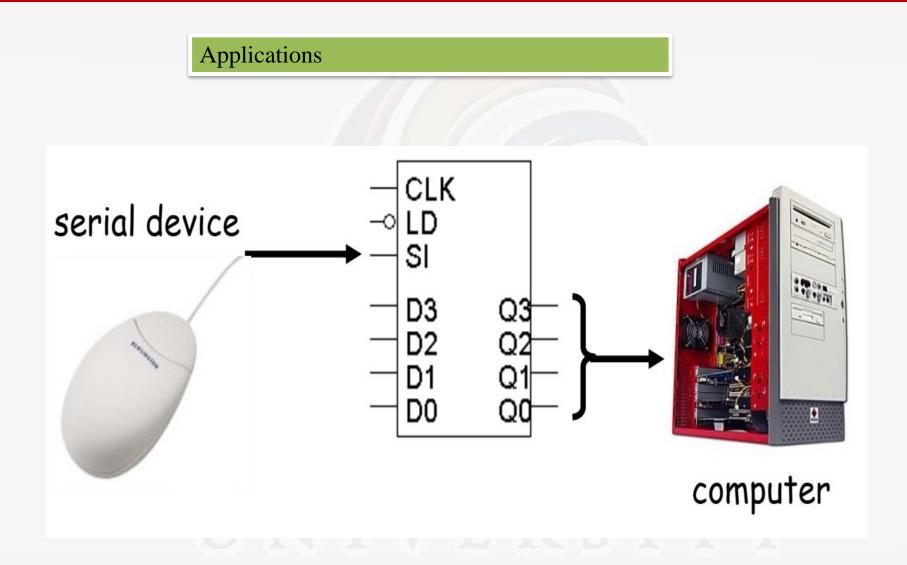
- Input devices such as keyboards and mice
- Output devices like printers
- Any serial port, USB or Firewire device transfers data serially
- Recent switch from Parallel ATA to Serial ATA in hard drives

To receive serial data using a shift register:

- The serial device is connected to the register's SI input
- The shift register outputs Q3-Q0 are connected to the computer
- The serial device transmits one bit of data per clock cycle
- These bits go into the SI input of the shift register
- After four clock cycles, the shift register will hold a four-bit word
- The computer then reads all four bits at once from the Q3-Q0 outputs.

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- Digital Fundamentals, Thomas L. Floyd, 11th Ed., 2015, Pearson Education Limited
- Modern Digital Electronics, R P Jain, 4th Ed., 2010, Tata McGraw Hill

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