synchronous counter and Decade Counter

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In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called **Synchronous counter**. In other words, changes in the output occur in "synchronisation" with the clock signal.

The result of this synchronisation is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

Binary 4-bit Synchronous Up Counter

It can be seen that the external clock pulses (pulses to be counted) are fed directly to each of the **J-K flip-flops** in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.
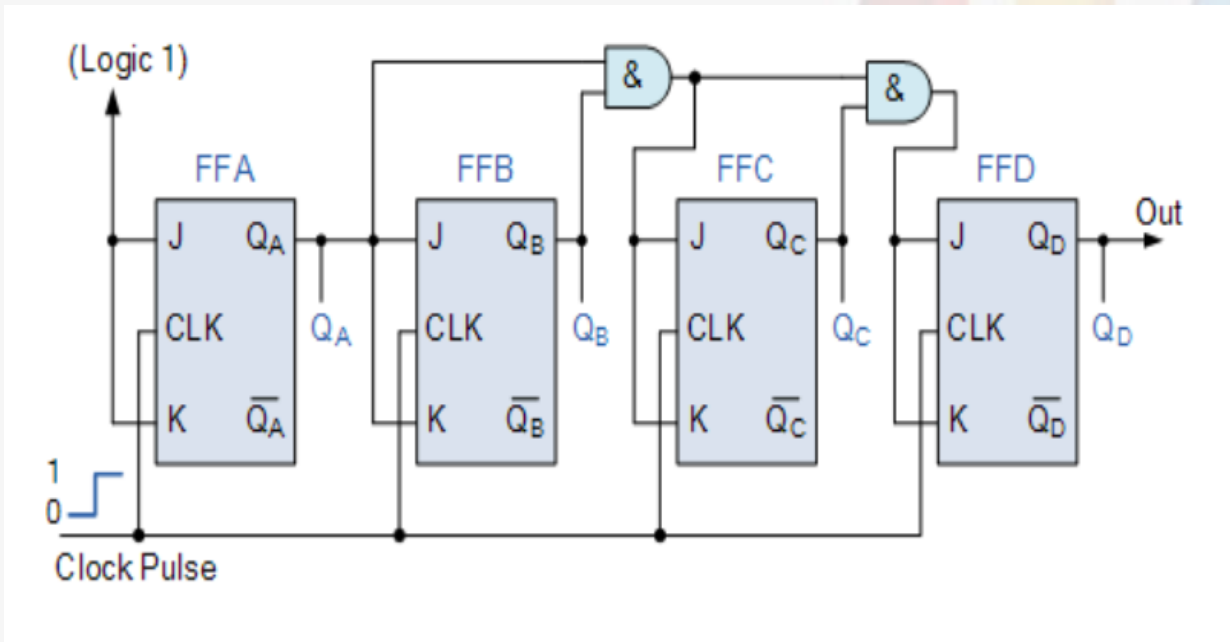
The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.

If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

4-bit Synchronous Counter Waveform Timing Diagram
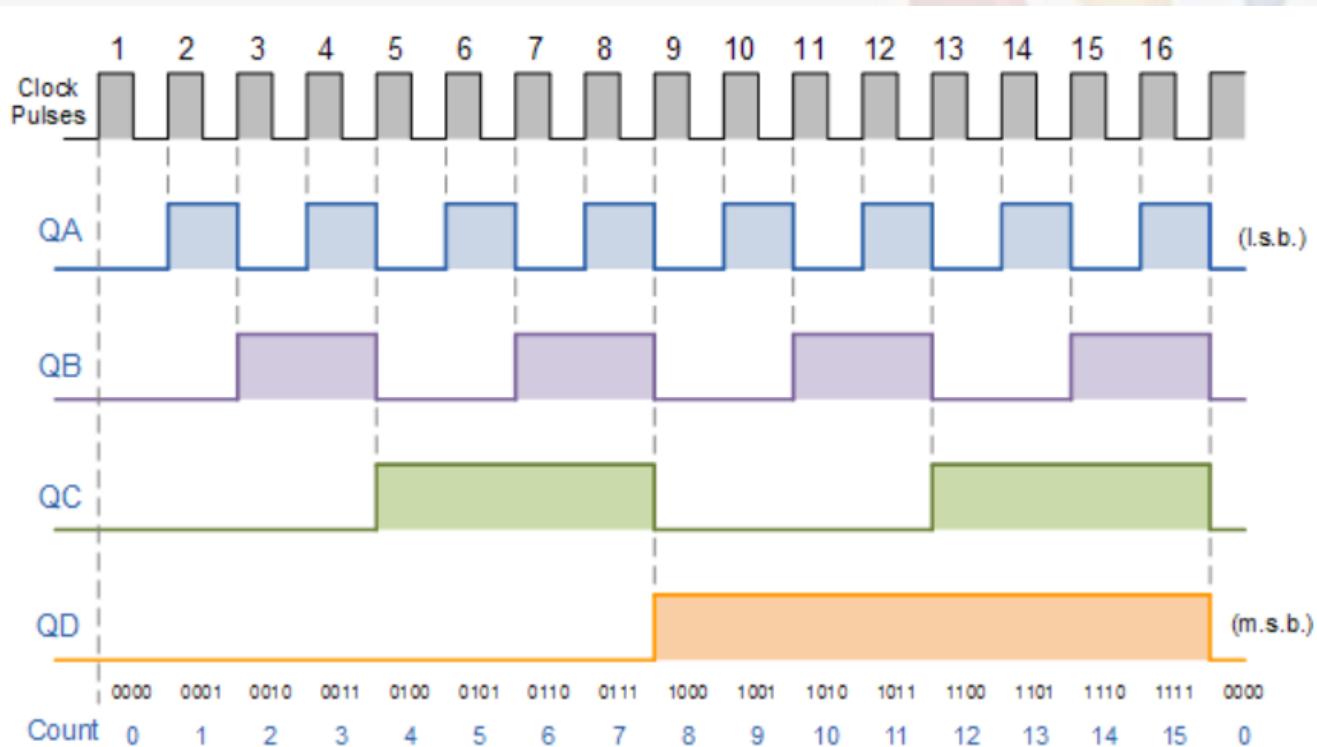
This 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111). Therefore, this type of counter is also known as a **4-bit Synchronous Up Counter**. However, we can easily construct a **4-bit Synchronous Down Counter** by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above. Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.

Binary 4-bit Synchronous Down Counter
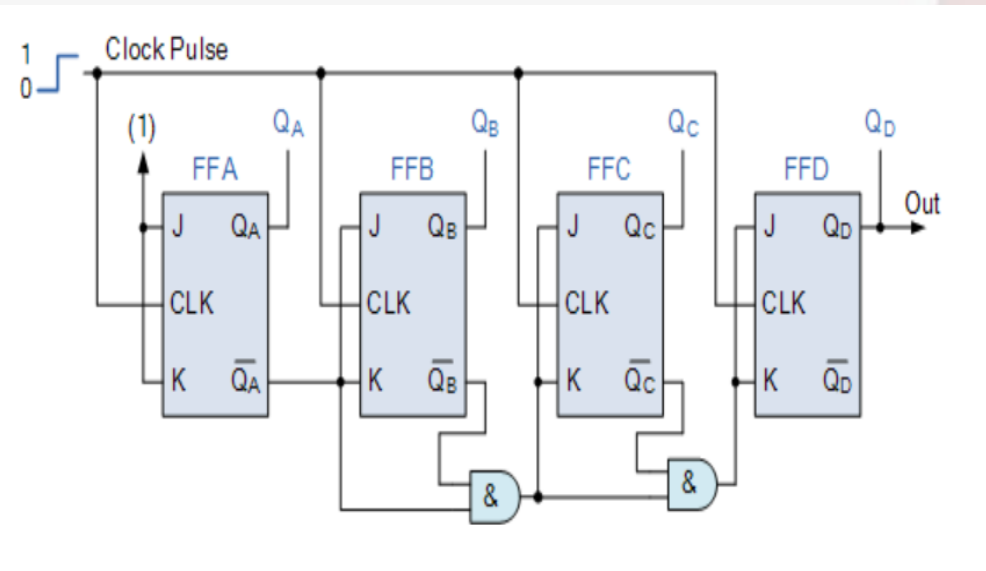
As synchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter, the modulo's or "MOD" number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences. All we need to increase the MOD count of an up or down synchronous counter is an additional flip-flop and AND gate across it.
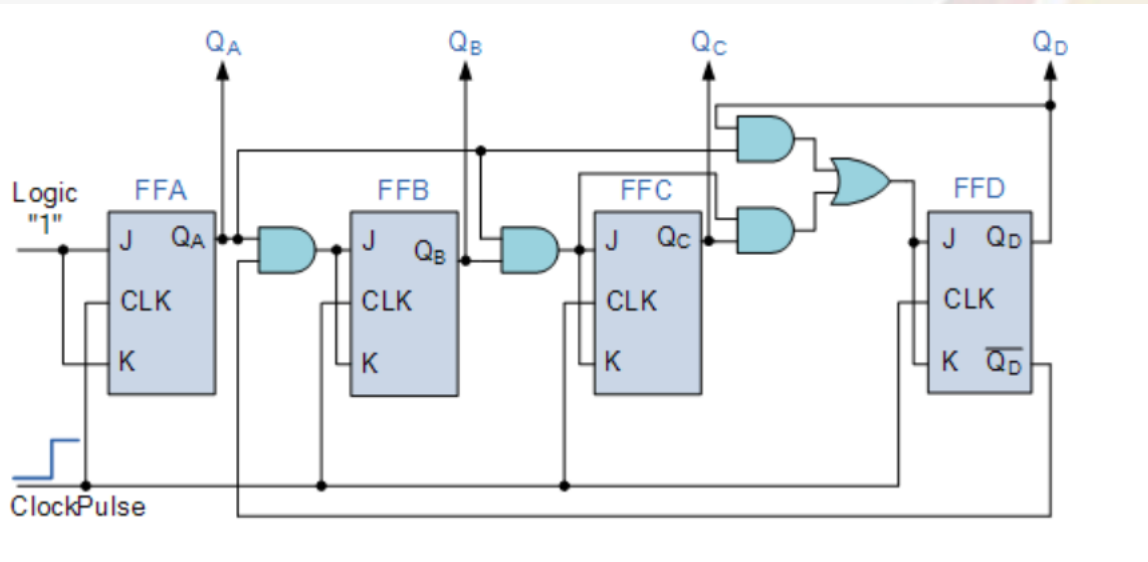
Decade 4-bit Synchronous Counter

A 4-bit decade synchronous counter can also be built using synchronous binary counters to produce a count sequence from 0 to 9. A standard binary counter can be converted to a decade (decimal 10) counter with the aid of some additional logic to implement the desired state sequence. After reaching the count of "1001", the counter recycles back to "0000". We now have a decade or **Modulo-10** counter.

Decade 4-bit Synchronous Counter

This counter is similar to synchronous counter but two AND gates were added more one OR gate. These gates are needed to be able to stop counting at 9 and loop back to 0.

The additional AND gates detect when the counting sequence reaches "1001", (Binary 10) and causes flip-flop FF3 to toggle on the next clock pulse. Flip-flop FF0 toggles on every clock pulse. Thus, the count is reset and starts over again at "0000" producing a synchronous decade counter.

We could quite easily re-arrange the additional AND gates in the above counter circuit to produce other count numbers such as a Mod-12 counter which counts 12 states from"0000" to "1011" (0 to 11) and then repeats making them suitable for clocks, etc.

Advantages and Disadvantage of Synchronous Counter

Now we are familiar with Synchronous counter and what are the difference between the Asynchronous counter and Synchronous counter. Synchronous counter eliminates lots of limitations which arrive in Asynchronous counter.
The **advantages of the Synchronous counter** is as follows-
1. It's easier to design than the Asynchronous counter.
2. It acts simultaneously.
3. No propagation delay associated with it.
4. Count sequence is controlled using logic gates, error chances are lower.
5. Faster operation than the Asynchronous counter.

Although there are many advantages, one major **disadvantage** of working with Synchronous counter is that it requires a lot of extra logic to perform.

Applications of Synchronous Counter

Few applications where Synchronous counters are used-
1. Machine Motion control
2. Motor RPM counter
3. Rotary Shaft Encoders
4. Digital clock or pulse generators.
5. Digital Watch and Alarm systems.

References:
- Digital Principles and Applications, A.P. Malvino, D. P. Leach and Saha, 7th Ed., 2011, Tata McGraw Hill
- Digital Fundamentals, Thomas L. Floyd, 11th Ed., 2015, Pearson Education Limited
- Modern Digital Electronics, R P Jain, 4th Ed., 2010, Tata McGraw Hill